REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Claims

Claim 1 has been amended to include the limitations of original claims 5 and 6, and to recite that the reconfigurable apparatus forms an adder, multiplier, or arithmetic logic unit. New claims 18-20 recite that the processing elements can be homogeneous, heterogeneous, or mixed.

The recitation of the adder, multiplier, and ALU is supported by, for example, page 4, lines 10-11 (ALU or multiplier); page 7, lines 22-24 (addition and multiplication configuration modes); page 8, lines 1-3 and Fig. 4 (adder); and page 8, lines 4-7 and Fig. 5 (multiplier). See also, by way of example, page 9, lines 6-7, 15-17 and page 11, lines 10-18. As a result, the additions to claim 1 do not constitute "new matter."

The recitations of homogeneous, heterogeneous, or combined units with same or different processing elements are supported by the above passages and also by page 3, lines 18-20 and 23-24. As a result, new claims 18-20 do not introduce "new matter."

The remaining changes to the claims are all formal in nature, including correction of the antecedence errors noted below, and therefore also do not constitute "new matter."

2. Rejection Under 35 USC §112, 2nd Paragraph

This rejection has been addressed by amending claims 15-17 to delete the references to "internal hardware components" and to positively recite multiple different function units, thereby correcting the antecedence errors noted in item 3 on page 2 of the Official Action.

3. Rejection of Claims 1 and 3-17 Under 35 USC §102(b) in view of U.S. Patent No. 6,226,735 (Mirsky)

This rejection is respectfully traversed on the grounds that the Mirsky patent fails to disclose or suggest a reconfigurable unit having a plurality of **4-bit processing elements** and a plurality of switch boxes, as claimed, that may be connected to form functional units such as an **ALU, multiplier**, or **adder**, as recited in claim 1, and in which the functional units may further be combined to form more complicated functional units having additional functions. The Mirsky patent, on the other hand, discloses processing elements that include, as described for example in col. 5, lines 21-59, a main memory in the form of "a group of ***256 eight bit SRAM cells*** that can operate in one of four modes" (col. 5, lines 34-35) as well as "three semi-independent functional blocks" which each "comprise an ***eight bit wide ALU*** 3002, an ***8x8 to sixteen bit ALU multiplier*** 3004, and a ***sixteen bit accumulator 3006***" (col. 5, lines 30-39). These elements of the processing elements of Mirsky hardly correspond to the claimed "4-bit processing elements" connected by switch boxes. Further, there is no suggestion that the individual components of the processing elements of Mirsky, such as the ALU 3002 or multiplier 3004 are themselves functional units made up of 4-bit processing elements connected by switch boxes. While Mirsky uses the "processing element" terminology, the processing elements of Mirsky, and the functional blocks that make up the processing elements, do not correspond to the claimed processing elements and functional units.

The present invention permit a functional unit configuration with the most hardware similarity to be found, and defines the most common hardware in the functional units as a processing element. According to the invention, two or more **4-bit processing elements** are combined using one or more switch boxes to form a functional unit that can be an adder, a multiplier, or an arithmetic logic unit. This solves the problem, described in the introductory section of the present application of being able to dynamically change hardware configurations while maximizing hardware utilization and therefore increasing computing efficiency, by compromising between the so-called "**fine-grain architecture**" which uses **1 or 2 bits**, and the "**coarse grain architecture**" using **8-bit** (or complete word) **processing elements**. The present

invention reduces hardware complexity relative to 1 or 2 bit designs while avoiding the problem of idling components when the "coarse grain architecture" is used to perform certain computations, as described in page 2, line24 to page 3, line 5 of Applicant's specification.

The **Mirsky** patent, in contrast, clearly discloses a **"coarse grain architecture"** having multiple **8-bit** data processing components rather than the claimed functional units, in which **4-bit** processing elements are connected by switch boxes to form adders, multipliers, and arithmetic logic units by appropriate control of the switch boxes. Thus, the processing elements and functional blocks of Mirsky are fundamentally different than, and do not correspond to, the processing elements and functional units of the claimed invention.

Because the Mirsky patent does not disclose all of the elements recited in the claims, withdrawal of the rejection of claims 1-17 under 35 USC §102(b) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

BACON & THOMAS, PLLC

By: BENJAMIN E. URCIA
Registration No. 33,805

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BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500